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MC68341

ADDENDUM TO
MC68341 Integrated Processor User's Manual

April 19, 1995

This addendum to the initial release of the MC68341UM/AD User's Manual provides corrections to the original text, plus additional information not included in the original. This document and other information on this product is maintained on the AESOP BBS, which can be reached at (800)843-3451 (from the US and Canada) or (512)891-3650. Configure modem for up to 14.4Kbaud, 8 bits, 1 stop bit, and no parity. Terminal software should support VT100 emulation. Internet access is provided by telneting to pirs.aus.sps.mot.com [129.38.233.1] or through the World Wide Web at http://pirs.aus.sps.mot.com.

1. Signal Index

On page 2-4, Table 2-4, the QSPI serial clock QSCLK should be listed as an I/O signal. At the bottom of Table 2-5, FC3/$\overline{\text{DTC}}$ is an output-only signal.

2. Operand Alignment

On page 3-9, last paragraph, change the first two lines to: "The CPU32 restricts all operands (both data and instructions) to be word-aligned. That is, word and long-word operands must be located on a word boundary." Long-word operands do not have to be long-word aligned.

3. $\overline{\text{WE}}$ on Fast Termination

On page 3-17, Figure 3-6, $\overline{\text{UWE}}$ and $\overline{\text{LWE}}$ do not assert for fast termination writes.

4. Write Cycle Timing Waveforms

On page 3-25, the M68300 write cycle timing diagram (Figure 3-12) shows incorrect timing for $\overline{\text{DS}}$, $\overline{\text{UWE}}$, and $\overline{\text{LWE}}$. On page 3-28, the M68000 write cycle timing diagram (Figure 3-14) shows incorrect timing for $\overline{\text{AS68K}}$, $\overline{\text{CSx}}$, $\overline{\text{UDS}}$/$\overline{\text{LDS}}$, and $\overline{\text{UWE}}$/$\overline{\text{LWE}}$. Replace these figures with the following corrected figures.

5. Additional Note on MBAR Decode

Add to the CPU Space Cycles description on page 3-31: The CPU space decode logic allocates the 256-byte block from $3FF00-3FFFF to the SIM module. An internal 2-clock termination is provided by this initial decode for any access to this range, but selection of specific registers depends on additional decode.

Accesses to the MBAR register at long word $3FF00 are internal only, and are only visible by enabling show cycles. Users should directly access only the MBAR register, and use the LPSTOP instruction to generate the LPSTOP broadcast access to $3FFFE. The remaining address range $3FF04-3FFFD is Motorola reserved and should not be accessed.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

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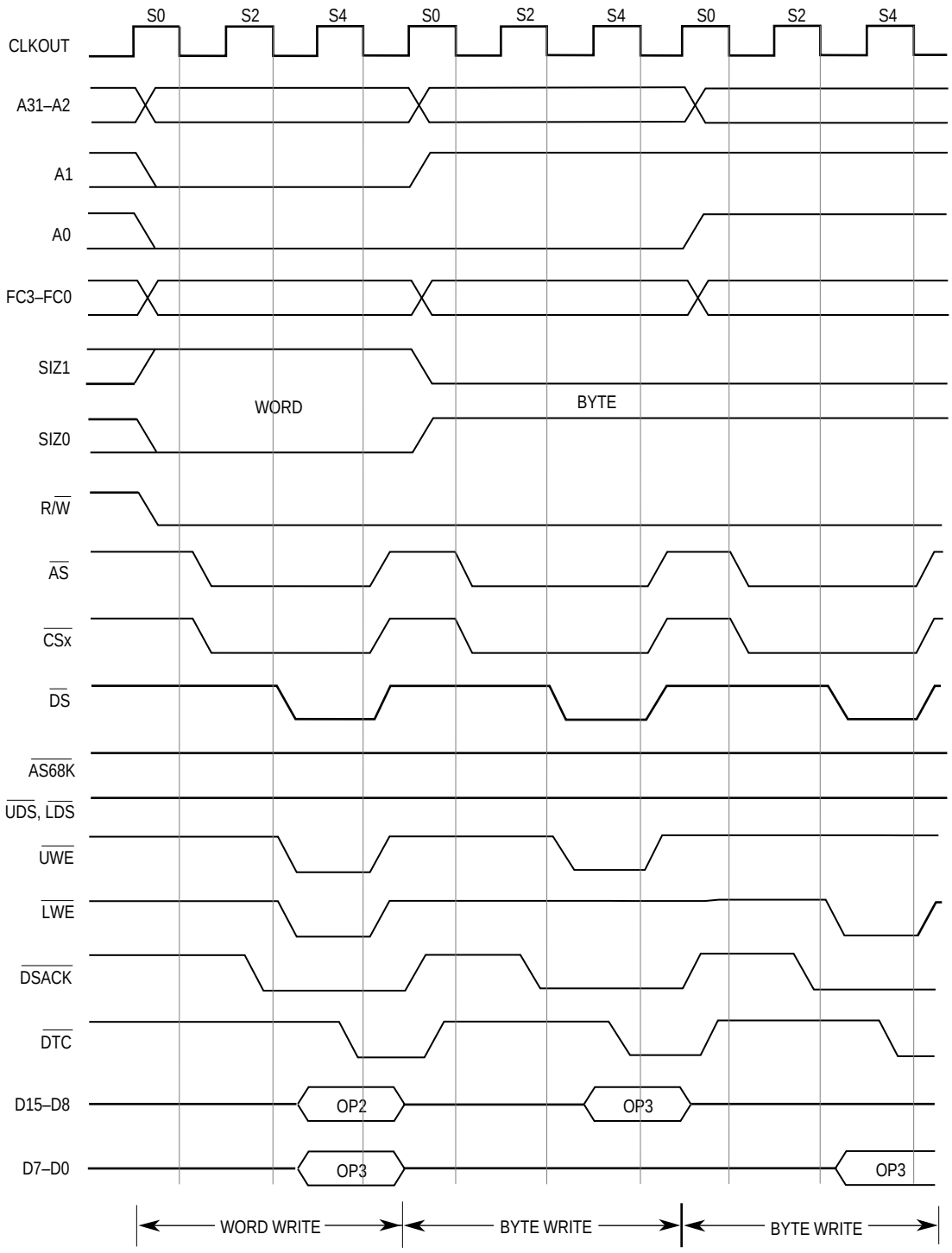


Figure 3-12. M68300 Write Cycle timing

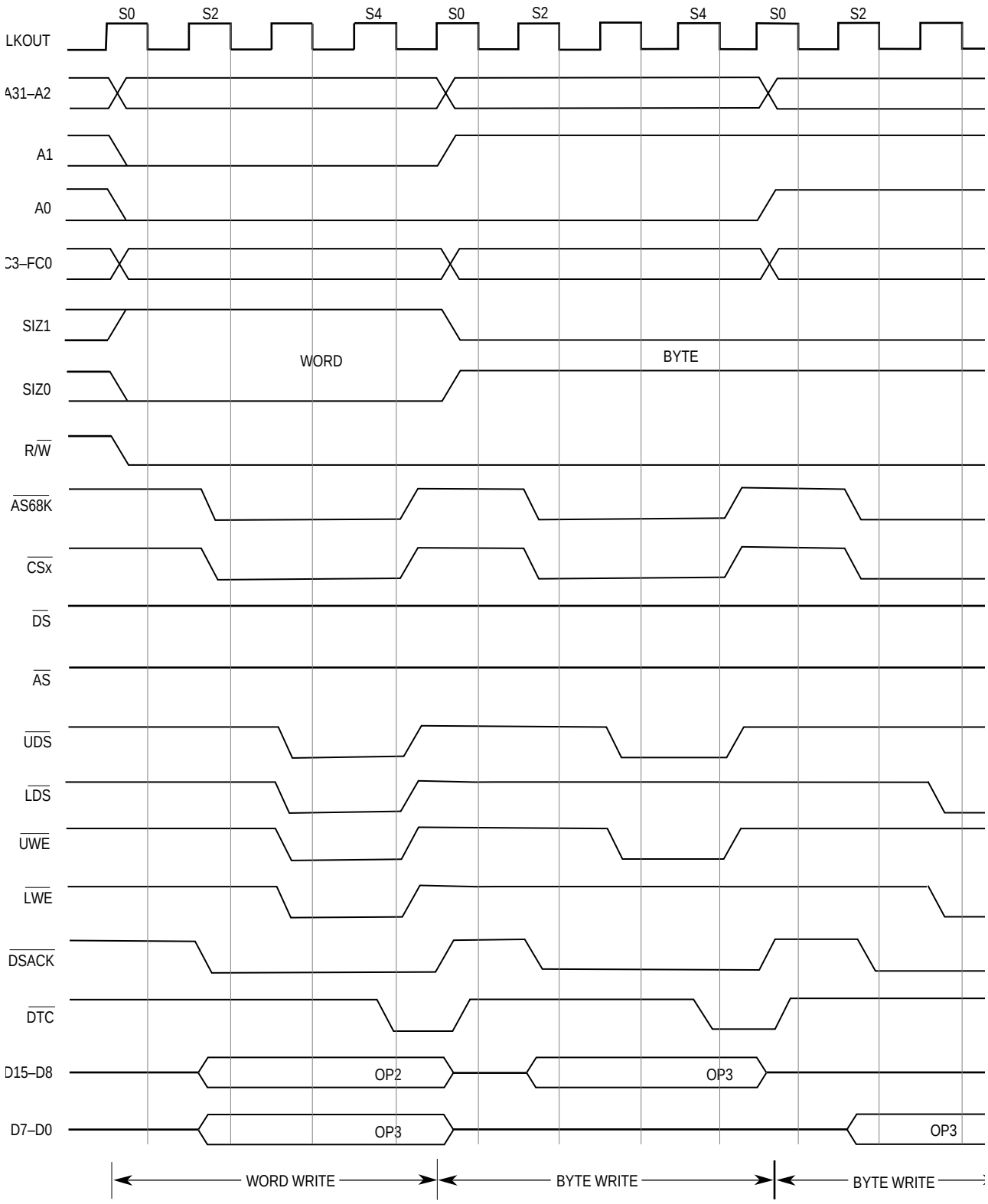


Figure 3-14. M68000 Write Cycle Timing

6. Additional Notes on CPU Space Address Encoding

On page 3-31, Figure 3-16, the BKPT field for the Breakpoint Acknowledge address encoding is on bits 4-2, and the T bit is on bit 1. The Interrupt Acknowledge LEVEL field is on bits 3-1.

7. Breakpoints

On page 3-31, the last paragraph implies that either a software breakpoint (BKPT instruction) or hardware breakpoint can be used to insert an instruction. As noted in the following paragraphs, only a software breakpoint can be used to insert an instruction on the breakpoint acknowledge cycle.

8. Interrupt Latency

Add to the Interrupt Acknowledge Bus Cycles section on page 3-36: Interrupt latency from $\overline{\text{IRQx}}$ assert to prefetch of the first instruction in the interrupt handler is about 37 clocks + worst case instruction length in clocks (using 2-clock memory and autovector termination). From the instruction timing tables, this gives 37+71 (DIVS.L with worst-case <fea>) = 108 clocks worst case interrupt latency time. For applications requiring shorter interrupt response time the latency can be reduced by using simpler addressing modes and/or avoiding use of longer instructions (specifically DIVS.L, DIVU.L, MUL.L).

9. Interrupt Hold Time and Spurious Interrupts

Add to the Interrupt Acknowledge Bus Cycles section on page 3-36: Level sensitive interrupts must remain asserted until the corresponding IACK cycle; otherwise, a spurious interrupt exception may result or the interrupt may be ignored entirely. This is also true for level sensitive external interrupts which are autovectored using either the $\overline{\text{AVEC}}$ signal or the AVEC register, since the SIM will not respond to an interrupt arbitration cycle on the IMB if the external interrupt at that level has been removed. External interrupts configured as edge sensitive only have to be held a minimum of 1.5 clocks - see section 4.3.5.8 PROGRAMMABLE INTERRUPT REGISTER (PIR).

Note that the level 7 interrupt is also level sensitive, and must be held until a level 7 IACK begins. The level 7 interrupt is unique in that it cannot be masked - another level 7 interrupt exception can be created after the IACK cycle by negating IRQ7 and reasserting, even though the interrupt mask level in the SR is now set to level 7.

10. Typos in IACK Cycle Timing Waveforms

On page 3-38, Figure 3-21, the text “VECTOR FROM 16-BIT PORT” should be on D7-D0, and “VECTOR FROM 8-BIT PORT” should be on D15-D8. The responding device returns the vector number on the least significant byte of the data port.

11. Additional Note on Internal Autovector Operation

Add to the Autovector Interrupt Acknowledge Cycle section on page 3-38: If an external interrupt level is autovectored either by the AVEC register programming or the external AVEC signal, an external IACK will be started and terminated internally. The interrupting device should not respond to this IACK in any way, or the resulting operation is undefined.

12. Additional Notes on Retry Termination

On page 3-42, Table 3-4: When $\overline{\text{HALT}}$ and $\overline{\text{BERR}}$ are asserted together in case #5 to force a retry of the current bus cycle, relative timing of $\overline{\text{HALT}}$ and $\overline{\text{BERR}}$ must be controlled to avoid inadvertently causing bus error ter-

mination case #3. This can be done by asserting $\overline{\text{HALT}}$ and $\overline{\text{BERR}}$ either synchronously to the clock to directly control which edge each is recognized on, or asynchronously with $\overline{\text{HALT}}$ asserted for time [spec 47A+spec 47B] ns before $\overline{\text{BERR}}$ to guarantee recognition on or before the same clock edge as $\overline{\text{BERR}}$.

13. Active Negate on Bus Arbitration

The 68341 actively pulls up all tri-stateable bus pins other than the data bus before tristating them during bus arbitration. This pullup function is not guaranteed to result in spec VOH levels before tristating, but will help reduce rise time on these signals when using weak external bus pullups.

14. Additional Note on Bus Arbitration Priority

For the bus arbitration description beginning on page 3-49: The arbitration priority between possible bus masters for this device is external request via $\overline{\text{BR}}$ (highest priority), DMA, then CPU (lowest). The priority of DMA channels 1 and 2 relative to each other is selected by their respective MAID levels which must be unique.

15. Additional Note on Bus Arbitration and Operand Coherency

For the bus arbitration description beginning on page 3-49: Each bus master maintains operand coherency when a higher priority request is recognized. For example, a CPU write of a long-word operand to a byte port results in a sequence of four bus cycles to complete the operand transfer - the CPU will not release the bus until the completion of the fourth bus cycle. A single address DMA transfer is handled in a similar manner. For a dual address DMA transfer, the read and write portions are handled as separate operands, allowing arbitration between the read and write bus cycles. Also, if different port sizes are specified in the DMA configuration for the source and destination, arbitration can occur between each of the multiple operand accesses which must be made to the smaller port for each operand access to the larger port. The RMC read/write sequences for a TAS instruction is also indivisible to guarantee data coherency. Arbitration is allowed between each operand transfer of a multi-operand operation such as a MOVEM instruction or exception stacking.

16. Additional Notes on RESET Interaction with Current Bus Cycle

Add to the Reset Operation description beginning page 3-55:

Hardware resets are held off until completion of the current operand transfer in order to maintain operand coherency. The processor resets at the end of the bus cycle in which the last portion of the operand is transferred, or after the bus monitor has timed out. The bus monitor operates for this specific case whether it is enabled or not, for the period of time that the BMT bits are set to.

The following reset sources reset all internal registers to their reset state: external, POR, software watchdog, double bus fault, loss of clock. Execution of a RESET instruction resets the peripheral module registers with the exception of the MCR registers. The MCR register in each module, the SIM41 registers, and the CPU state are not affected by execution of a RESET instruction.

17. External Reset

On page 3-56, Figure 3-33, the $\overline{\text{RESET}}$ signal negates for two clocks between internal and external assertions, not one. Note that $\overline{\text{RESET}}$ is not actively negated, and its rise time is dependent on the pullup resistor used.

18. Power-On Reset

On page 3-57, Figure 3-34. Power-Up Reset Timing Diagram: CLKOUT is not gated by VCO lock or other internal control signals, and can begin toggling as soon as VCC is high enough for the internal logic to begin operating. For crystal mode and external clock with VCO mode, after the VCO frequency has reached an initial

stable value, the 328*TCLKIN delay is counted down, and VCO lock is set after completion of the 328 clock delay. For external clock mode without VCO, the 328*TCLKIN delay starts as soon as EXTAL clock transitions are recognized. See note for page11-3 for more POR information.

19. Internal IMB Arbitration

On page 4-6, first paragraph, change the first sentence to read “There are eight arbitration levels for the various bus masters on the MC68341 to access the inter-module bus (IMB).”

20. Additional Note for External Clock Mode with PLL

On page 4-9, Table 4-1, External Clock Mode with PLL: the PLL phase locks the CLKOUT falling edge to the falling edge of the EXTCLK input clock. Maximum skew between falling edges of the EXTCLK and CLKOUT signals is specified in the Section 12 Electrical Characteristics.

21. External Clock Mode Operation

The next-to-last paragraph on page 4-11 incorrectly states that the SYNCR V, W, X, Y, and Z bits can all affect the system frequency in external clock mode. In external clock mode only the V bit affects the system frequency, by selecting either EXTCLK or EXTCLK/2 as reference input to the phase comparator. The VCO frequency divided by 2 is used both for CLKOUT as well as the feedback input to the phase comparator. A reset forces V=0, resulting in an initial processor operating frequency of 1/2 the EXTCLK frequency.

For applications using external clock mode, the 32KHz crystal connected to EXTAL and XTAL is only required if the realtime clock function is needed - ground EXTAL if the RTC is not used. Also, the clock input on EXTCLK should be very clean when the 32KHz oscillator is used. Excessive undershoot or overshoot, as well as fast edge rates may result in coupling to the adjacent XTAL input, affecting operation of the 32kHz oscillator.

22. Recommended XFC Capacitor Values

On page 4-12, third paragraph, and page 11-2, last paragraph: The XFC capacitor recommendation of 0.01µF to 0.1µF applies specifically to crystal mode operation. When using external clock with VCO mode, for phase detector refernce frequencies > 1MHz start with a capacitance value of 10000pf/F_MHz. For example at 16.0MHz the recommended XFC capacitance is approximately 10000pf/16.0 = 625pf - choose the next higher standard value available.

23. CLKOUT and VCO Frequency Programming

On pages 4-13 and 4-14, the column for W=1:Z=0:X=1 is incorrect - the correct value for each entry in this column is 2x the frequency in the X=0 column immediately to the left. A corrected table is shown on the following pages. Note that although a complete table is shown for all W:X:Y:Z combinations, both CLKOUT and VCO frequency limits must be observed when programming the SYNCR. For example, a system operating frequency (CLKOUT) of 25.16MHz can be selected with W:X:Y:Z=1:1:23:1, resulting in a VCO frequency of 50.3MHz. However, programming W:X:Y:Z=1:0:47:1 to achieve the same system frequency would result in a VCO frequency of greater than 100MHz, which is outside the spec VCO frequency operating range.

24. Additional Note for Global Chip Select

On page 4-16, section 4.2.4.2: When operating as a global chip select, CS0 does not assert for accesses to either the MBAR or to internal peripheral module registers.

Table 4-2. System Frequencies from 32.768-kHz Reference

	CLKOUT (kHz)				VCO (kHz)	CLKOUT (kHz)				VCO (kHz)
	W = 0				W = 0	W = 1				W = 1
	Z = 0		Z = 1		Z = x	Z = 0		Z = 1		Z = x
Y	X = 0	X = 1	X = 0	X = 1	X = x	X = 0	X = 1	X = 0	X = 1	X = x
0	16	33	131	262	524	66	131	524	1049	2097
1	33	66	262	524	1049	131	262	1049	2097	4194
2	49	98	393	786	1573	197	393	1573	3146	6291
3	66	131	524	1049	2097	262	524	2097	4194	8389
4	82	164	655	1311	2621	328	655	2621	5243	10486
5	98	197	786	1573	3146	393	786	3146	6291	12583
6	115	229	918	1835	3670	459	918	3670	7340	14680
7	131	262	1049	2097	4194	524	1049	4194	8389	16777
8	147	295	1180	2359	4719	590	1180	4719	9437	18874
9	164	328	1311	2621	5243	655	1311	5243	10486	20972
10	180	360	1442	2884	5767	721	1442	5767	11534	23069
11	197	393	1573	3146	6291	786	1573	6291	12583	25166
12	213	426	1704	3408	6816	852	1704	6816	13631	27263
13	229	459	1835	3670	7340	918	1835	7340	14680	29360
14	246	492	1966	3932	7864	983	1966	7864	15729	31457
15	262	524	2097	4194	8389	1049	2097	8389	16777	33554
16	279	557	2228	4456	8913	1114	2228	8913	17826	35652
17	295	590	2359	4719	9437	1180	2359	9437	18874	37749
18	311	623	2490	4981	9961	1245	2490	9961	19923	39846
19	328	655	2621	5243	10486	1311	2621	10486	20972	41943
20	344	688	2753	5505	11010	1376	2753	11010	22020	44040
21	360	721	2884	5767	11534	1442	2884	11534	23069	46137
22	377	754	3015	6029	12059	1507	3015	12059	24117	48234
23	393	786	3146	6291	12583	1573	3146	12583	25166	50332
24	410	819	3277	6554	13107	1638	3277	13107	26214	52429
25	426	852	3408	6816	13631	1704	3408	13631	27263	54526
26	442	885	3539	7078	14156	1769	3539	14156	28312	56623
27	459	918	3670	7340	14680	1835	3670	14680	29360	58720
28	475	950	3801	7602	15204	1901	3801	15204	30409	60817
29	492	983	3932	7864	15729	1966	3932	15729	31457	62915
30	508	1016	4063	8126	16253	2032	4063	16253	32506	65012
31	524	1049	4194	8389	16777	2097	4194	16777	33554	67109

Table 4-2. System Frequencies from 32.768-kHz Reference (Continued)

	CLKOUT (kHz)				VCO (kHz)	CLKOUT (kHz)				VCO (kHz)
	W = 0				W = 0	W = 1				W = 1
	Z = 0		Z = 1		Z = x	Z = 0		Z = 1		Z = x
Y	X = 0	X = 1	X = 0	X = 1	X = x	X = 0	X = 1	X = 0	X = 1	X = x
32	541	1081	4325	8651	17302	2163	4325	17302	34603	69206
33	557	1114	4456	8913	17826	2228	4456	17826	35652	71303
34	573	1147	4588	9175	18350	2294	4588	18350	36700	73400
35	590	1180	4719	9437	18874	2359	4719	18874	37749	75497
36	606	1212	4850	9699	19399	2425	4850	19399	38797	77595
37	623	1245	4981	9961	19923	2490	4981	19923	39846	79692
38	639	1278	5112	10224	20447	2556	5112	20447	40894	81789
39	655	1311	5243	10486	20972	2621	5243	20972	41943	83886
40	672	1343	5374	10748	21496	2687	5374	21496	42992	85983
41	688	1376	5505	11010	22020	2753	5505	22020	44040	88080
42	705	1409	5636	11272	22544	2818	5636	22544	45089	90178
43	721	1442	5767	11534	23069	2884	5767	23069	46137	92275
44	737	1475	5898	11796	23593	2949	5898	23593	47186	94372
45	754	1507	6029	12059	24117	3015	6029	24117	48234	96469
46	770	1540	6160	12321	24642	3080	6160	24642	49283	98566
47	786	1573	6291	12583	25166	3146	6291	25166	50332	100663
48	803	1606	6423	12845	25690	3211	6423	25690	51380	102760
49	819	1638	6554	13107	26214	3277	6554	26214	52429	104858
50	836	1671	6685	13369	26739	3342	6685	26739	53477	106955
51	852	1704	6816	13631	27263	3408	6816	27263	54526	109052
52	868	1737	6947	13894	27787	3473	6947	27787	55575	111149
53	885	1769	7078	14156	28312	3539	7078	28312	56623	113246
54	901	1802	7209	14418	28836	3604	7209	28836	57672	115343
55	918	1835	7340	14680	29360	3670	7340	29360	58720	117441
56	934	1868	7471	14942	29884	3736	7471	29884	59769	119538
57	950	1901	7602	15204	30409	3801	7602	30409	60817	121635
58	967	1933	7733	15466	30933	3867	7733	30933	61866	123732
59	983	1966	7864	15729	31457	3932	7864	31457	62915	125829
60	999	1999	7995	15991	31982	3998	7995	31982	63963	127926
61	1016	2032	8126	16253	32506	4063	8126	32506	65012	130023
62	1032	2064	8258	16515	33030	4129	8258	33030	66060	132121
63	1049	2097	8389	16777	33554	4194	8389	33554	67109	134218

NOTES:

1. Some W/X/Y/Z bit combinations shown may select a CLKOUT or VCO frequency higher than spec. Refer to **Section 11 Electrical Characteristics** for CLKOUT and VCO frequency limits.
2. Any change to W or Y results in a change in the VCO frequency - the VCO should be allowed to relock if necessary.

25. Additional Note on PORTA/B Output Timing

Add to the External Bus Interface Operation description on page 4-17: The Port A and Port B output pins transition after the S4 falling edge for the internal write to the respective data register. This places port pin transitions at roughly the same time DS negates for the data register write - note this output delay is not currently specified in the Electrical Specifications.

26. RTC Memory Map

The RTC register offsets shown on page 4-21 are incorrect - a corrected memory map is shown below. Addresses within the RTC can be accessed as either bytes or words, with the exception of the reserved byte at offset $0CE. Note that RTC registers marked S/U are read/write in supervisor mode, but can only be read in user mode.

ADDR	FC	15 8	ADDR	FC	7 0
0C0	S	RTC INTERRUPT CONTROL (RICR)			
0C2	S/U	MINUTES (MIN)	0C3	S/U	SECONDS (SEC)
0C4	S/U	DATE	0C5	S/U	HOUR
0C6	S/U	MONTH	0C7	S/U	YEAR
0C8	S	RTC CONTROL/STATUS (RCR)	0C9	S/U	DAY
0CA	S/U	MINUTES ALARM (MINA)	0CB	S/U	SECONDS ALARM (SECA)
0CC	S/U	DATE ALARM (DATEA)	0CD	S/U	HOURS ALARM (HOURA)
0CE	-	RESERVED	0CF	S	RTC CALIBRATION (RCCR)

27. MBAR Register Reset Values

On page 4-22, the reset values for MBAR bits 31-12 are undefined.

28. MBAR AS7 Bit and IACK Cycles

On page 4-23, the second code sequence initializes the MBAR register with AS7 set. This prevents the address decode for the internal 4K register block from responding to CPU space accesses. In particular, it prevents the register block decode of $FFFFFxxx from interfering with IACK cycles (address $FFFFFFFx), and possibly corrupting the vector number returned. Normal interrupt acknowledge operation for the internal modules is not affected by this change.

Early versions of the MC68330 User's Manual (original release) and MC68340 User's Manual (original and Rev. 1 releases) did not show AS7 set. Code which was developed based on these manual revisions should be checked for this problem when porting to the MC68341 - this change should also be applied back to the MC68330 and/or MC68340.

29. Additional Note on VCO Overshoot

On page 4-30 place the following note under the Y-bits description:

A VCO overshoot can occur when increasing the operating frequency by changing the Y bits in the SYNCR register. The effects of this overshoot can be controlled by following this procedure:

1. Write the X bit to zero. This will reduce the previous frequency by one half.
2. Write the Y bits to the desired frequency divided by 2.
3. After the VCO lock has occurred, write the X bit to one. This changes the clock frequency to the desired frequency.

Steps 1 and 2 may be combined.

30. RCCR Initialization

Add to the RCCR description on page 4-41: the RCCR register is unaffected by a processor reset, and contains an arbitrary value on initial powerup of the RTC. Calibration software should clear the RCCR register before beginning the calibration process, since RTC operation with an invalid RCDx value is undefined. RCCR[7] is reserved - on current silicon it always reads 0, and should always be written 0.

31. RCCR Typos

On page 4-42, delete the first description for RCD4-RCD0 near the top of the page.

32. MONTH Register Range

The valid range for the MONTH register on page 4-43 is 1-12, with “1” corresponding to January and “12” corresponding to December.

33. SIM41 Example Code

On page 4-49, about mid-page, change “MOVEQ #8-1,D0” to “MOVEQ #16-1,D0” to initialize all 8 chip selects.

34. Bus Error Stack Frame

On page 5-61, in the next-to-last paragraph, delete “(the internal transfer count register is located at SP+$10 and the SSW is located at SP+12)”. The stack space allocation is the same for both faults - the location of the internal count register and SSW remains the same. The only difference is that the faulted instruction program counter location SP+10 and SP+12 will contain invalid data. To tell the difference between the two stack frames, look at the first nibble of the faulted exception format vector word located at SP+$E - it will be $0 for the four-word frame, and $2 for the six-word frame.

35. DSO Timing

On page 5-71, Figure 5-23, DSO transitions one clock later than shown.

36. Typo on BDM RSREG Command

On page 5-77, Section 5.6.2.8.6, RSREG register bit #8 should be a “1”.

37. $\overline{\text{IPIPE}}$ Timing

On page 5-88, Figure 5-29 shows the third $\overline{\text{IPIPE}}$ assertion low lasting for 1.5 CLKs - it actually asserts for an additional 0.5 CLKs. $\overline{\text{IPIPE}}$ transitions occur after the falling edge of CLKOUT.

38. Additional Notes on DMA Features

In the feature set listed on page 6-1, bullet six is “Operand Packing and Unpacking for Dual-Address Transfers”. This packing is for transfers between different port sizes selected in the DMA channel control register, e.g. Byte <> Word transfers. The DMA controller does not do packing for byte > byte transfers, eliminating the problem of residual bytes left in the controller when a channel is stopped after an odd byte transfer count.

39. Additional Note on Internal Request Generation

Add to the Internal Request Generation section on page 6-5: For internal request operation, $\overline{\text{DACKx}}$ and $\overline{\text{DONEx}}$ are not active as outputs during transfers. $\overline{\text{DONEx}}$ is valid as an input though and will terminate channel operation if asserted - pull up if not used.

40. Additional Note on DMA Transfer Latency from $\overline{\text{DREQ}}$

Add to the External Request Generation section beginning 6-5: $\overline{\text{DREQx}}$ assertions require two clocks for input synchronization and IMB bus arbitration activity before the resulting DMA bus cycle can start. A $\overline{\text{DREQx}}$ assertion will preempt the next CPU bus cycle if it is recognized two or more clocks before the end of the current bus cycle, unless the current cycle is not the last cycle of an operand transfer, or is the read of an RMC cycle. Operand transfers and RMC read/write sequences are indivisible to guarantee data coherency - the bus cannot be arbitrated from the CPU until the complete operand transfer completes, even if operand and memory sizing results in multiple bus cycles.

For a $\overline{\text{DREQx}}$ assertion during an idle bus period, bus state S0 of the DMA bus cycle starts 2.5 clocks after the clock falling edge which $\overline{\text{DREQx}}$ is recognized on. The maximum latency from the clock falling edge that $\overline{\text{DREQx}}$ is recognized on to the falling edge that $\overline{\text{AS}}$ for the DMA cycle asserts from is shown in the following table for various memory speeds.

DREQ Latency (Clocks) vs. Bus Width and Access Times

Access Type	Maximum $\overline{\text{DREQ}}$ Latency (Clocks)							
	16-Bit Bus Clocks/Bus Cycle				8-Bit Bus Clocks/Bus Cycle			
	2	3	4	5	2	3	4	5
Longword	7	9	11	13	11	15	19	23
RMC (TAS)	10	12	14	16	10	12	14	16

41. Additional Note on Burst Transfer $\overline{\text{DREQx}}$ Negation and Overhead

On page 6-5, replace the 2nd paragraph of 6.3.2.1 External Burst Mode with the following: $\overline{\text{DREQx}}$ must be negated one clock before the end of the last DMA bus cycle of a burst to prevent another DMA transfer from being generated. Also, $\overline{\text{DREQx}}$ must be negated two clocks before the end of the last DMA bus cycle to prevent an idle clock between that transfer and the following CPU access.

42. Additional Note on Cycle steal DMA arbitration overhead

Add to the External Cycle Steal Mode description on page 6-6: In general, DMA arbitration occurs transparently. However, for some 2-clock accesses using cycle steal an idle clock can follow the DMA transfer due to incomplete overlap of the DMA transfer with internal IMB arbitration. Specifically, an idle clock can follow 1) single address 2-clock transfers and 2) dual address transfers from memory to 2-clock devices. Arbitration is completely overlapped for all other cases.

43. Additional Note on Cycle Steal

For the external cycle steal mode description on page 6-6, the initial $\overline{\text{DREQx}}$ assertion does not have to be held off until after the channel is started. If $\overline{\text{DREQx}}$ is already asserted when the channel is started by setting the channel start bit, an internal $\overline{\text{DREQx}}$ assertion is generated, providing the edge needed for the DMA cycle to start.

44. $\overline{\text{DREQx}}$ Negation on Burst

On page 6-8, Figure 6-5, and on page 6-10, Figure 6-7, $\overline{\text{DREQx}}$ should negate before the falling edge of S2 (one clock earlier than shown) to prevent another DMA transfer from occurring. See the note above for page 6-5 on Burst Transfer $\overline{\text{DREQx}}$ Negation.

45. $\overline{\text{DREQ}}$ Assert Time

On page 6-21, Figure 6-13: The second $\overline{\text{DREQx}}$ assertion should be shown held for an additional clock to guarantee recognition on 2 consecutive clock falling edges. The figure shows it as just being 1 clock period. Note 1 should be deleted.

46. Fast Termination and Burst Request Mode

On the last paragraph of page 6-21, delete the reference to Figure 6-14. Figure 6-14 on page 6-22 is labeled incorrectly - it actually shows operation with fast termination, cycle steal, and dual address transfers. Also, the second $\overline{\text{DREQx}}$ signal should be held for 2 consecutive falling edges - the figure shows it being held for only 1 clock edge. Note 1 of Figure 6-14 should be deleted.

47. Typo in DAPI

On page 6-26, for DAPI = 1, the DAR is incremented according to the destination size (not the source size).

48. Additional note on DMA limited rate operation

On page 6-27, in the BB-Bus Bandwidth Field: The DMA “active” count increments only when the DMA channel is the bus master (each channel has its own counter). If a higher priority bus master forces the channel to relinquish the bus before completion of the active count, the counter stops until the channel regains the bus. Higher priority requests could come from 1) the other DMA channel (if it has a higher MAID level), 2) the CPU32 core (if either the interrupt mask level in the SR or the interrupt request level is higher than the DMA channel's ISM level), or 3) an external bus request. When the active count is exhausted, the DMA channel releases the bus, and the “idle” count increments regardless of bus activity.

49. Configuration Error

The Configuration Error description paragraph at the top of page 6-29 should be replaced with “A configuration error results when 1) either the SAR or DAR contains an address that does not match the port size specified in the CCR, or 2) the BTC register does not match the larger port size or is zero.”

50. Additional Note on DMA Interrupt Prioritization

Add to the Interrupt Register description on page 6-31: When both DMA channels are programmed to the same interrupt level, channel 1 is higher priority than channel 2.

51. Single Address Enable

6-33 SE-Single Address Enable: The note “used for intermodule DMA” should be for the SE=1 case. The 68341 does not support intermodule single address transfers, so the SE bit should always be programmed to “0”.

52. Code Examples - Immediate Addressing Mode

On pages 6-40 through 6-44 make the following change as shown for each occurrence of SARADD, DARADD, and NUMBYTE (change to immediate addressing mode for source operand):

MOVE.L SARADD,DMASAR1(A0) should be MOVE.L #SARADD,DMASAR1(A0).

MOVE.L DARADD,DMADAR1(A0) should be MOVE.L #DARADD,DMADAR1(A0).

MOVE.L NUMBYTE,DMABTC1(A0) should be MOVE.L #NUMBYTE,DMABTC1(A0).

53. Serial Oscillator Problems with DMA activity

Add to the Crystal Input or External Clock (X1) section on page 7-5: A high $\overline{\text{DREQ1}}$ request rate (greater than 1MHz) with excessive undershoot on $\overline{\text{DREQ1}}$ can result in internal signal coupling to the serial module oscillator X1 pin, damping out oscillation. Avoid routing $\overline{\text{DREQ1}}$ near the serial oscillator external components, and use termination techniques such as series termination of the $\overline{\text{DREQ1}}$ driver (start with 33Ω) to limit edge rate of the signal and accompanying undershoot.

54. Additional Note on $\overline{\text{RTSx}}$ operation details

Add to the $\overline{\text{RTSA}}$ and $\overline{\text{RTSB}}$ descriptions on page 7-6: The $\overline{\text{RTSx}}$ outputs are active low signals - they drive a logic “0” when set, and a logic “1” when cleared.

$\overline{\text{RTSx}}$ can be set (output logic level 0) by any of the following:

- Writing a “1” to the corresponding bit in the OPSET register $71E
- Issuing an “Assert RTS” command using command register CR
- If RxRTS=1, set by receiver FIFO transition from FULL to not-FULL

$\overline{\text{RTSx}}$ can be cleared (output logic level 1) by any of the following:

- Hardware reset of the serial module
- Writing a “1” to the corresponding bit in the OPRESET register $71F
- Issuing a “Negate RTS” command using command register CR
- If RxRTS=1, cleared by receiver FIFO transition from not-FULL to FULL
- If TxRTS=1, cleared by completion of last character, including transmission of stop bits

55. Serial Frequency Restriction

On page 7-8, place the following notes at the end of **Section 7.3.1 Baud Rate Generator**:

The current implementation of the serial module restricts the minimum CLKOUT frequency at which the baud rate generators can be used to approximately 8.3MHz. Operation below this frequency results in a synchronized internal clock which is at a lower frequency than the X1 input, which then results in incorrect baud rates. One method to extend the minimum CLKOUT frequency is to reduce the X1 frequency by powers of 2 as shown in the table below. The corresponding baud rates selected by the clock select register programming are

scaled by the same factor. This method preserves most of the standard baud rates (19200, 9600, 4800, etc.).

Serial XTAL Frequency	CLKOUT F_{min}	Max Availabile Baud Rate
3.6864MHz	8.29MHz	76.8k
1.8432	4.15	38.4k
0.9216	2.07	19.2k

CLKOUT min = 2.25*XTAL frequency

Alternatively, the baud rate clock can be supplied directly through the SCLK input. Since there is a single SCLK input, both serial channels must use the same baud rate clock, although one could be clocked in the 1x mode and the other in the 16x mode. When using this method, the X1 input can be tied to ground - no crystal is required.

56. 68341 Serial Module RTS Difference from 68681

Add to the description for receiver-controlled RTS operation in the next-to-last paragraph on page 7-13: Unlike the 68681, the RTSx signal does not have to be manually asserted the first time in the mode to support control-flow capability on the receiver.

57. Additional Note on Serial multidrop operation

Add to the Multidrop Mode section beginning on page 7-15: For multidrop mode, it is not necessary to disable the transmitter to manipulate the A/D bit, as generally implied in the manual, nor is it necessary to wait until the previous character completes transmission (i.e. TxEMP). The serial module logic latches this bit and appends it to the data character when the character is transferred from the transmit buffer to the serial output shift register. Once this transfer occurs (as indicated by the TxRDY assertion), the A/D bit in MR1 can be changed without affecting the character in progress. The proper programming sequence to change the A/D bit for the next character would be:

1.) poll TxRDY until asserted (or interrupt on TxRDY)

2.) set/clear A/D bit in MR1 for new character

3.) write character to transmit buffer (TB)

4.) A/D bit can be changed only after TxRDY asserts again

No other bits in MR1 should be modified when changing the A/D bit.

58. Typo in CPE Description

The CPE bit header on page 8-20 should be "Counter/Prescaler Enable".

59. Typo in Status Register Configuration

On page 8-26, Section 8.5.1, the Status Register (SR) description should say: "• Clear the TO, TG, and TC bits to reset the interrupts."

60. Typos in Timer Initialization Examples

On pages 8-27 and 8-29, the Timer register offsets should be from the timer base address, not from the SIM41 base address. The correct equates for the Timer register offsets are:

```
* Timer register offsets from timer1 base address
IR      EQU       $4   interrupt register
CR      EQU       $6   control register
SR      EQU       $8   status register
CNTR    EQU       $A   counter register
PRLD1   EQU       $C   preload register 1
COM     EQU       $10  compare register
```

On page 8-27, change the last code line from "CLR.W SR(A0)" to "ORI.W #$7000,SR(A0)". The TO, TG, and TC interrupt status bits are cleared by writing a "1" to the corresponding bit, allowing individual bits to be cleared without affecting the other bits.

On page 8-28, second code line down, the "MOVE.W #$020F,IR(A0)" initializes the interrupt vector to the Uninitialized vector - change the $0F to a user-definable vector number. Repeat this correction on page 8-29, just past mid-page.

61. MC68341 BSDL File

An electronic copy of the BSDL file for the MC68341 is maintained on the AESOP BBS - refer to the beginning of this document for information on accessing AESOP.

62. Additional Note on Oscillator Layout Guidelines

Add to the Processor Clock Circuitry (page 11-1) and Serial Interface (page 11-4) sections: In general, use short connections and place external oscillator components close to the processor. Do not route other signals through or near the oscillator circuit, especially high frequency signals like CLKOUT, $\overline{AS}$, and $\overline{DREQ1}$ (see note above on $\overline{DREQ1}$ and serial oscillator for page7-5). Place a ground shield around the oscillator logic; use a separate trace for ground to the oscillator so that it does not carry any of the digital switching noise.

63. Recommended 32KHz Oscillator Circuit

On page 11-2, Figure 11-2, a 10M resistor can be substituted for the 20M R2 bias resistor as shown below.

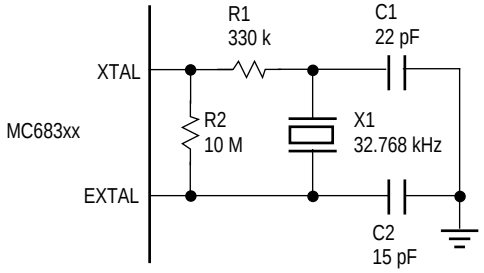


Figure 11-2. Sample Crystal Circuit

64. SRAM Interface

The SRAM interface shown in Figure 11-5 on page 11-4 does not support 2-clock accesses, since $\overline{UWE}$ and $\overline{LWE}$ do not assert for 2-clock writes.

65. Corrections to 8/16-Bit DMA Control Logic

On page 11-10, the logic driving $\overline{OE}$ on the 74F245 in Figure 11-14 should be corrected as shown below. Although not detailed, the byte enables for the memory block should be controlled during reads to prevent contention between the upper and lower bytes of the data bus when D7-D0 is muxed to the upper data byte.

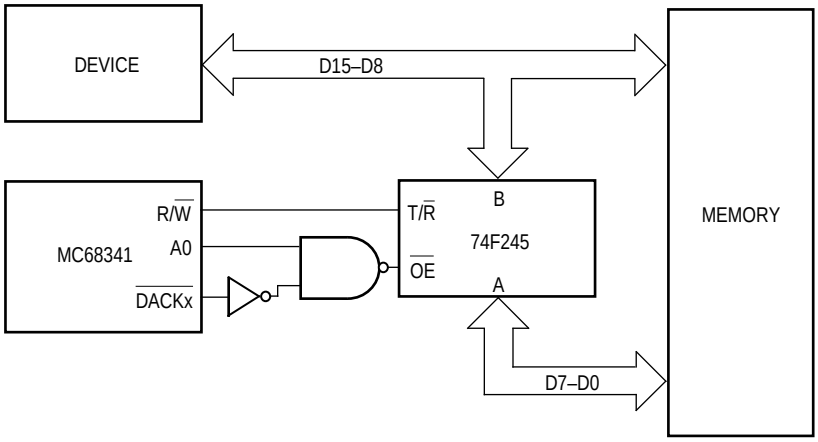


Figure 11-14. Circuit For Interfacing 8-Bit Device to 16-Bit Memory in Single-Address DMA Mode

66. X1 and $\overline{BSW}$ Input Levels

On page 12-5, the Clock Input High Voltage spec also applies to the X1 and $\overline{BSW}$ inputs.

67. Operating IDD Limits

On page 12-5, the spec operating (RUN) currents are shown in the following table:

Product	Frequency	Max Idd	Typical IDD (25°C)
68341FT16V	16.78MHz	95mA@3.6V	68mA@3.3V
68341FT16	16.78MHz	150mA@5.25V	121mA@5.0V
68341FT25	25.16MHz	210mA@5.25V	175mA@5.0V

68. Input Clock Duty Cycle in External Clock w/PLL mode

On page 12-7, External Clock With PLL Mode: The input clock 20/80% duty cycle for external clock with PLL mode can be used when the VCO is not turned off during LPSTOP. During LPSTOP with the VCO turned off, the input clock is used for clocking the SIM, and must meet the tighter duty cycle requirements outlined for External Clock Mode Without PLL.

69. Clock Skew Notes

12-7, External Clock With PLL Mode, Clock Input to CLKOUT Skew: Clock skew is measured from the falling

edges of the clock signals - the PLL phase locks the falling edge of CLKOUT to the falling edge on EXTCLK.

70. Data Setup Time for 3.3V

On page 12-9, electrical specification #27 (Data Setup to CLKOUT Low) for 3.3V product only has been changed from 5ns to 8ns.

71. $\overline{\text{UWE}}$ and $\overline{\text{LWE}}$ Signals

In Figure 12-3 on page 12-12, $\overline{\text{UWE}}$ and $\overline{\text{LWE}}$ will assert for the write buys cycle with the same timing as $\overline{\text{DS}}$. In the fast termination write cycle in Figure 12-5 on page 12-14, $\overline{\text{UWE}}$ and $\overline{\text{LWE}}$ (not shown) remain negated like $\overline{\text{DS}}$.

72. Serial Module Specs

Note 1 on page 12-25 should reference synchronous operation, not asynchronous.

73. Ordering Information

Replace the the ordering information table in Section 11 with the following ordering information.

Supply Voltage	Package Type	Frequency (MHz)	Temperature	Order Number
5.0 V	Plastic Quad Flat Pack FT Suffix	0 – 25	0°C to +70°C -40° to 85°C	XC68341FT25 XC68341CFT25
5.0 V	Plastic Quad Flat Pack FT Suffix	0 – 16.78	0°C to +70°C -40° to 85°C	XC68341FT16 XC68341CFT16
3.3 V	Plastic Quad Flat Pack FT Suffix	0 – 16.78	0°C to +70°C	XC68341FT16V

74. Upper and Lower Data Strobes

In paragraph 3.2.8 page 3-6, change (D15–D0) to (D15–D8) and (D8–D0) to (D7–D0).

75. Figure 3-2

Change Note 1 to reference MC68341 instead of MC68340.

76. Figure 4-8

The Periodic Interrupt Control Register (PICR) and Periodic Interrupt Timing Register (PITR) should be 1 word instead of 2 bytes. Disregard the Scale Select Register.

77. Page 4-24

Refer to 4-17 for more information on the AVEC-Automatic Vector Responsibility.

78. Page 4-48

The lake at the start of the code should be INIT341 instead of INIT340.

79. Page 6-5, Paragraph 6.3.1.2

The table reference in the last sentence should be 6-4 not 6-5.

80. Page 9-19,

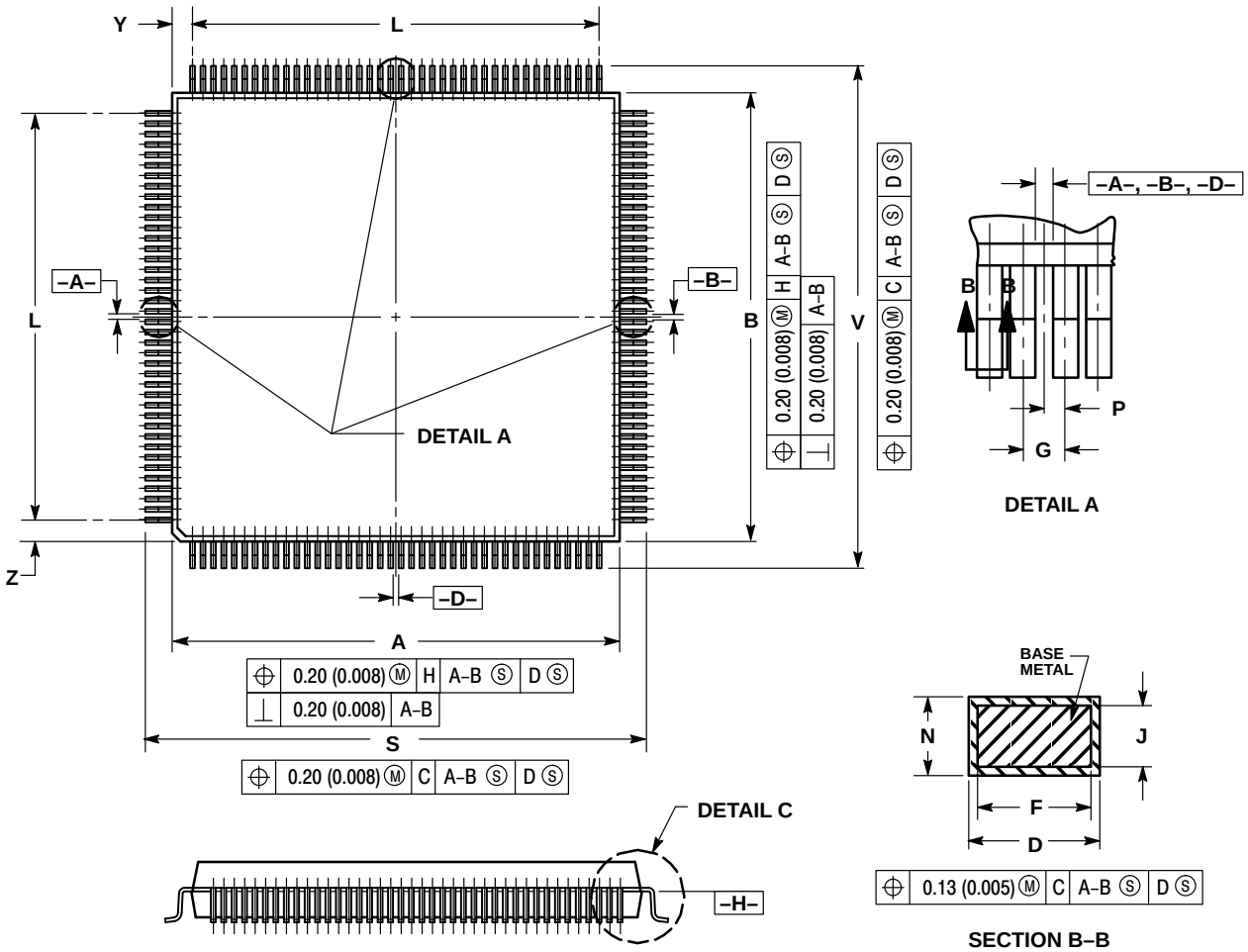
The timing diagrams reference as Figures 9-24 — 9-27 should be changes to 12-22–12-25.

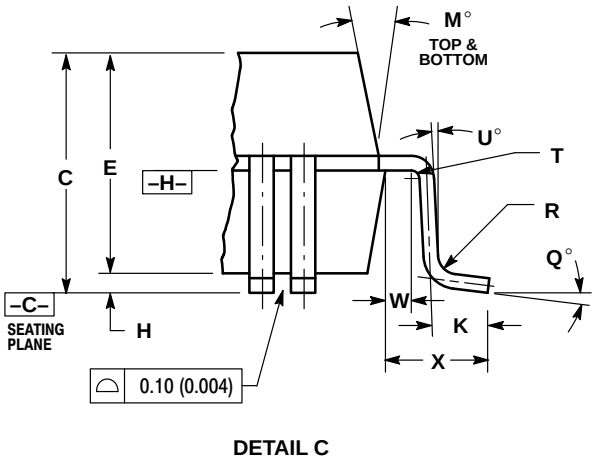
81. Page 9-29, DT–Delay

A value of 1 enable this bit and 0 disables it.

82. Package Dimensions

The package dimension drawing on page 13-3 should be discarded and replaced with the following drawing.





DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –A–, –B– AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –C–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.90	28.10	1.098	1.106
B	27.90	28.10	1.098	1.106
C	3.35	3.85	0.132	0.152
D	0.22	0.38	0.009	0.015
E	3.20	3.50	0.126	0.138
F	0.22	0.33	0.009	0.013
G	0.65 BSC		0.026 REF	
H	0.25	0.35	0.010	0.014
J	0.11	0.23	0.004	0.009
K	0.70	0.90	0.028	0.035
L	25.35 REF		0.998 REF	
M	5°	16°	5°	16°
N	0.11	0.19	0.004	0.007
P	0.325 BSC		0.013 BSC	
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	31.00	31.40	1.220	1.236
T	0.13	---	0.005	---
U	0°	---	0°	---
V	31.00	31.40	1.220	1.236
W	0.40	---	0.016	---
X	1.60 REF		0.063 REF	
Y	1.33 REF		0.052 REF	
Z	1.33 REF		0.052 REF	

Case 864A-03

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